REMARKS

This paper responds to the Office Action mailed on June 1, 2007.

Claims 1, 4, 9 and 46 are amended, no claims are canceled, and no claims are added; as a result, claims 1-6 and 8-50 are now pending in this application.

Information Disclosure Statement

Applicant submitted a Supplemental Information Disclosure Statement and a 1449 Form on March 7, 2007. The Examiner indicates that the documents are classified in unrelated classes and appear to be unrelated. The Applicant has not reviewed these documents and defers to the expertise of the Examiner as it appears that he has reviewed the documents to some extent. However, Applicant respectfully requests that an initialed copy of the 1449 Form be returned to Applicant's Representatives to indicate that the cited references have been considered by the Examiner.

§102 Rejection of the Claims

Claims 46-50 were rejected under 35 U.S.C. § 102(b) for anticipation by Lee et al. (KR Publication 2001-037699). Applicant respectfully traverses this rejection.

Lee discloses increasing total capacitance without increasing the aspect ratio (see abstract lines 1-2). The method has four oxide and two nitride layers, as compared to the present application's two oxide layers. Lee dry etches part of the fourth oxide 120 and second nitride 110 layers to expose the storage node contact 100, deposits polysilicon (11 in figure 1C and 130 in the abstract figure) on the sides of the fourth oxide 120 and fills the holes with a liquid spin on glass 12 (see lines 11-14 and figure 1C). An etch back results in a smooth top surface with the horizontal portions of the polysilicon exposed, which is then etched to separate the polysilicon 130 inside the storage node contact holes into separate capacitor plates, but still totally in contact with the fourth oxide 120 (or 10 in figures 1 and 2).

Applicant respectfully suggests that Lee's sidewalls are drawn as being vertical for simplicity, and not because the disclosed process results in vertical sidewalls. Applicant respectfully submits that Lee's disclosed order of dry and then wet etching, teaches away from the recited wet then dry etching of the present application. Applicant further notes that the

Examiner admitted in the prior Office Action that Lee's structure does not extend from the substrate that the recess was formed in, but rather is always surrounded by and in contact with the fourth oxide layer (10 in figure 1 or 120 in figure 2). Thus, the taught process of Lee is different and the resulting structure of Lee is different from the claimed invention.

Specifically, Applicant respectfully submits that the cited reference does not disclose at least the feature of "*...forming a recess in a first dielectric stack including a first dielectric layer on a substrate and a second dielectric layer formed of a material different from the first dielectric layer; forming a conductive structure in the recess, wherein the conductive structure has vertical sidewalls, is partially embedded in the recess, and wherein the conductive structure is formed to extend above a remaining portion of the first dielectric stack...*", as recited in independent claim 46, as amended herein, from which claims 47-50 directly depend. Lee forms the conductive structure 130 on the inside walls of the fourth oxide 120, and does not remove the fourth oxide, nor does any portion of the conductive structure extend above the fourth oxide 120. The present claimed arrangement as shown in figures 1F,1G, 3F and 3G has the conductive structure 132 or 352 extending above at least the first dielectric layer 138 or 339. Thus the process is different at least in extending above a remaining portion of the first dielectric stack, in having a different etch order, and in having sidewall recited to be vertical.

In view of the above noted differences in the claimed method, Applicant submits that the cited reference does not disclose each and every claimed feature, and thus the independent claim, as amended herein, are patentably distinct over the reference. The dependent claims are held to be patentably distinct over the cited reference at least as depending from base claims shown above to be patentable. Applicant respectfully requests this rejection be reconsidered and withdrawn.

§103 Rejection of the Claims

Claims 1-5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee et al. (KR Publication 2001-037699) in view of Choi (U.S. 6,080,594) and O'Brien (U.S. 5,817,182). Applicant respectfully traverses this rejection.

The cited reference of Lee discloses increasing total capacitance without increasing the aspect ratio (abstract lines 1-2). Lee dry etches part of the fourth oxide 120 and second nitride

110 layers to expose the storage node contact 100, deposits polysilicon (11 in figure 1C and 130 in the abstract figure) on the sides of the fourth oxide 120 and fills the holes with a liquid spin on glass 12 (see lines 11-14 and figure 1C). An etch back planarizes the top surface with the top of the polysilicon exposed, which is then etched into separate capacitor plates, but still in contact with the fourth oxide 120 (or 10 in figures 1 and 2).

The cited Choi reference is used in the outstanding Office Action to show that it is known to eliminate spin-on-glass by wet etching first. Lee teaches the importance of using a dry etch first, and thus the two references are in conflict and could provide no possible motivation to make the suggested combination.

The cited reference of O'Brien disclosing removal of etch residues, and is used in the outstanding Office Action to show that it is useful to rinse after etching in order to remove etchant residues that may impact subsequent processing, device yield or reliability.

Applicant submits that neither Choi nor O'Brien cure the above noted failure of Lee to teach or suggest vertical walls, or removing the fourth oxide from the outside of the non-vertical walls of the conductive structure, or to have a two layer dielectric stack that is etched.

Specifically, Applicant respectfully submits that the suggested combination of references fails to describe or suggest at least the features of "*...forming a first dielectric layer on a substrate; forming a second dielectric layer on the first dielectric layer; forming a first recess having a first lateral dimension at a bottom portion of the first dielectric layer in contact with the substrate, and having a second lateral dimension at a top portion of the second dielectric layer; forming a conductive structure in the first recess having vertical sidewalls with the first lateral dimension having a value approximately equal to a value of the second lateral dimension; first wet etching to expose a first portion of the conductive structure by removing at least a portion of the second dielectric layer... second non-wet etching to expose a second portion of the conductive structure by removing at least a remaining portion of the first dielectric layer and exposing at least a portion of the substrate...*", as recited in independent claim 1, as amended herein, with similar feature in claim 4, as amended herein, and from which claims 2-3 and 5 depend. The suggested combination of cited references do not describe or suggest having the conductive structure etched away from the support of the surrounding dielectric, nor do they suggest the recited order of etches used to obtain actual vertical sidewalls.

The independent claims have been shown above to have features not described or suggested by the suggested combination of references, and are thus held to be in patentable condition. The dependent claims are held to be patentable at least as depending from a patentable base claim, as shown above, since any claim depending from a nonobvious independent claim is also nonobvious. See M.P.E.P. § 2143.03. In view of the failure of the suggested combination of references to describe or suggest an etch process resulting in more vertical sidewalls and having conductive structures extending beyond the dielectric layer, Applicant respectfully requests this rejection under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Claims 6 and 8-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee et al. in view of Choi, O'Brien and Kang et al. (U.S. Publication 2004/0175884). Applicant respectfully traverses this rejection.

Lee discloses increasing total capacitance without increasing the aspect ratio, by dry etching the fourth oxide 120 and second nitride 110 layers to expose the storage node contact 100, depositing polysilicon 130 on the sides of the fourth oxide 120, and filling with spin on glass 12 (see lines 11-14 and figure 1C). An etch back planarizes the top surface of the polysilicon and etched into separate capacitor plates. The capacitor plates are still in contact with the fourth oxide 120.

Choi discloses that it is known to eliminate spin-on-glass by wet etching before dry etching, which teaches against the Lee teaching of the importance of using a dry etch first. The two references are in conflict and can not provide any possible motivation to make the suggested combination.

O'Brien discloses removal of etch residues, and shows that it is useful to rinse after etching in order to remove etchant residues that may impact subsequent processing, device yield or reliability.

The Kang reference discloses capacitors with a larger diameter at the bottom than at the middle of the capacitor, since Kang's figures show that the side walls 280 of the capacitor are outwardly sloping. Applicant submits that Kang's sidewalls are not vertical as recited in the present claims.

Applicant submits that no combination of the cited references can cure the above noted failure of Lee to teach or suggest either capacitor walls extending above the surrounding dielectric support, or the proper order of etching to obtain vertical side walls, or removing the fourth oxide from the outside of the non-vertical walls of the conductive structure, or having a two layer dielectric stack, or he use of the straightening etch shown in figure 1C (see pages 7 and 8). Applicant respectfully submits that Kang has no suggestion about nearly vertical capacitor walls, and thus the combination of Kang with the other cited references would not result in the present method and arrangement.

Applicant respectfully submits that the suggested combination of references fails to describe or suggest at least the features of "*...forming a first dielectric layer on a substrate; forming a second dielectric layer on the first dielectric layer; forming a first recess having a first lateral dimension at a bottom portion of the first dielectric layer in contact with the substrate, and having a second lateral dimension at a top portion of the second dielectric layer; forming a conductive structure in the first recess having vertical sidewalls with the first lateral dimension having a value approximately equal to a value of the second lateral dimension; first wet etching to expose a first portion of the conductive structure by removing at least a portion of the second dielectric layer... second non-wet etching to expose a second portion of the conductive structure by removing at least a remaining portion of the first dielectric layer and exposing at least a portion of the substrate...*", as recited in independent claim 1, as amended herein, with similar language in claim 9, from which claims 6 and 8, and claims 10-21 respectively depend. The suggested combination of references, whether taken alone or in any combination, does not suggest a method having the conductive structure etched away from the support of the initially surrounding dielectric, and thus the claims are patentable over the combination.

In view of the above claim amendments and discussion, Applicant submits that the independent claims have been shown to have recited features not described or suggested by the combination of cited references, and are thus in patentable condition. The dependent claims are held to be patentable at least as depending from a patentable base claim, as shown above, since any claim depending from a nonobvious independent claim is also nonobvious. See M.P.E.P. § 2143.03. In view of the failure of the suggested combination of references to describe or suggest an etch process resulting in more vertical sidewalls and having conductive structures extending

beyond the dielectric layer, Applicant respectfully requests this rejection under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Claims 40-45 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee et al. in view of Jost et al. (U.S. 5,966,611) and Sell (U.S. Publication 2004/0147074). Applicant respectfully traverses this rejection.

Lee discloses increasing total capacitance without increasing the aspect ratio, by dry etching the fourth oxide 120 and second nitride 110 layers to expose the storage node contact 100, depositing polysilicon 130 on the sides of the fourth oxide 120, and filling with spin on glass 12 (see lines 11-14 and figure 1C). An etch back planarizes the top surface of the polysilicon and etched into separate capacitor plates. The capacitor plates are still in contact with the fourth oxide 120.

Jost is used in the outstanding Office Action to show that organic sacrificial layers are known. The cited reference of Sell is used in the outstanding Office Action to show that trench capacitors are known to have aspect ratios.

Applicant respectfully submits that the suggested combination of references fails to describe or suggest at least the features of "*...stripping amorphous carbon from a conductive structure embedded therein having vertical sidewalls, wherein the conductive structure is coupled to a substrate active area, and wherein the conductive structure includes an aspect ratio from about 6:1 to about 25:1 ...*", as recited in independent claim 40, from which claims 41-45 depend. No combination of the cited references suggest removing amorphous carbon from a conductive structure embedded therein, such at the film 138 completely surrounding the container capacitor conductive structure 132 of figure 1F. Jost at col. 3, line 45, discloses removing a covering layer and not a layer having an embedded conductive structure as recited.

In view of the above discussion, Applicant submits that the independent claims have been shown to have recited features not described or suggested by the combination of cited references, and are thus in patentable condition. The dependent claims are held to be patentable at least as depending from a patentable base claim, as shown above, since any claim depending from a nonobvious independent claim is also nonobvious. See M.P.E.P. § 2143.03. In view of the failure of the suggested combination of references to describe or suggest an etch process

resulting in more vertical sidewalls and having conductive structures extending beyond the dielectric layer, Applicant respectfully requests this rejection under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Claims 22-39 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Chan et al. (U.S. 6,764,947) in view of O'Brien. Applicant respectfully traverses this rejection.

Chan discloses a method for reducing gate conductor line deformation due to thermal mismatch between the underlying dielectric layer and the polysilicon gate electrode, and between the polysilicon and an overlaying amorphous carbon hard mask due to lattice mismatch. The lattice mismatch may cause delamination of the amorphous hard mask formed above the polysilicon (col. 1, line 35). Chan solves the lattice mismatch by adding a silicon dioxide layer 20 between the polysilicon 18 and the amorphous carbon layer 22 (col. 3, line 16).

O'Brien is used to show that rinsing is a known process. Applicant respectfully submits that the suggested combination of references fails to suggest a process to form conductive structure that extend above the dielectric layers in which they were formed.

Applicant respectfully submits that the suggested combination of references fails to describe or suggest at least the features of "*...first etching a sacrificial second film to expose a first vertical portion of a conductive structure ...*", as recited in independent claims 22 and 29, from which the other claims depend. The cited references do not expose any vertical section of the conductor.

In view of the above discussion, Applicant submits that the independent claims have been shown to have recited features not described or suggested by the combination of cited references, and are thus in patentable condition. The dependent claims are held to be patentable at least as depending from a patentable base claim, as shown above, since any claim depending from a nonobvious independent claim is also nonobvious. See M.P.E.P. § 2143.03. In view of the failure of the suggested combination of references to describe or suggest an etch process resulting in more vertical sidewalls and having conductive structures extending beyond the dielectric layer, Applicant respectfully requests this rejection under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

RESERVATION OF RIGHTS

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicants respectfully submit that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicants' attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By their Representatives,

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Date 27 Aug '07

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this _27th_ day of August 2007.

Name

Signature